

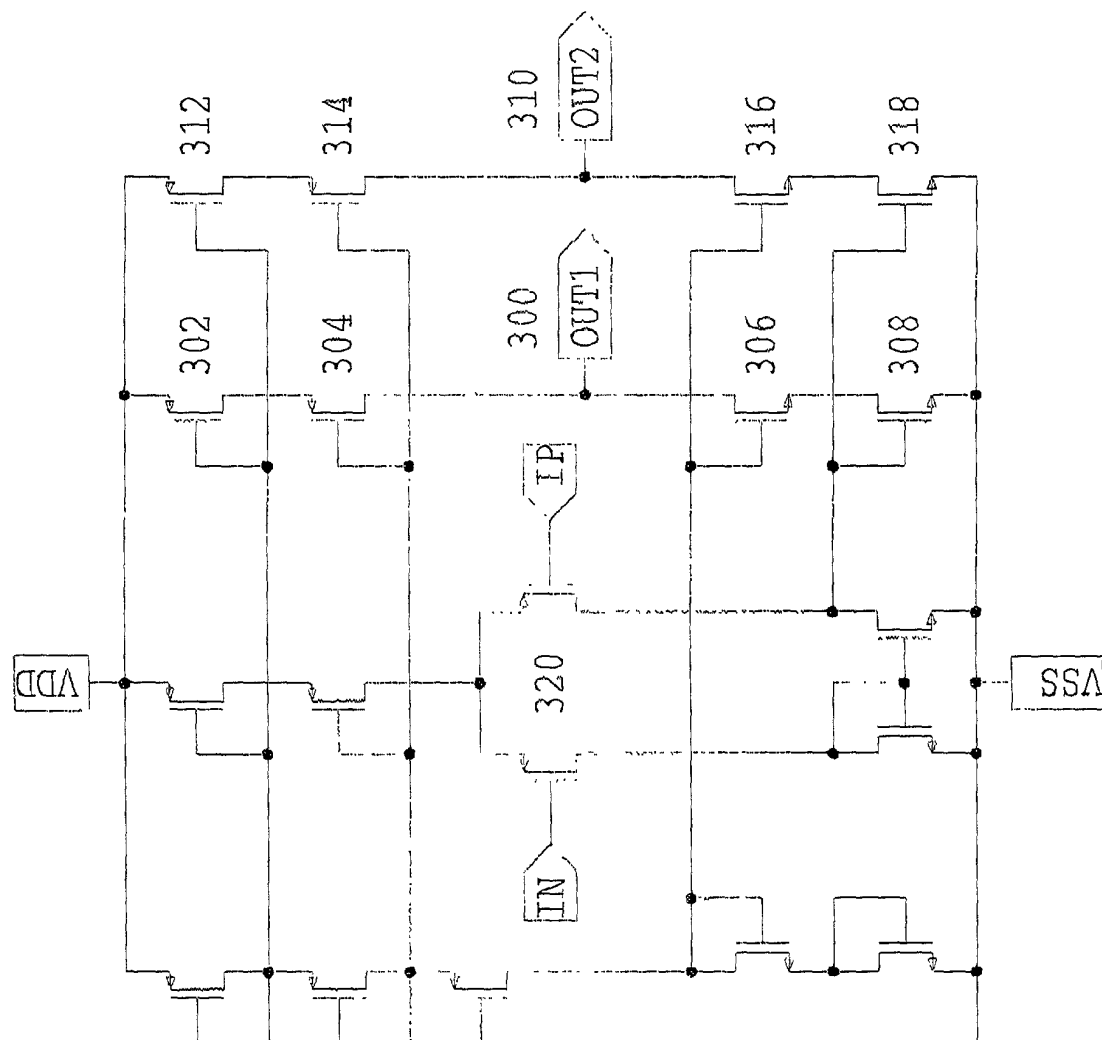
[illegible]

FIGURE 3

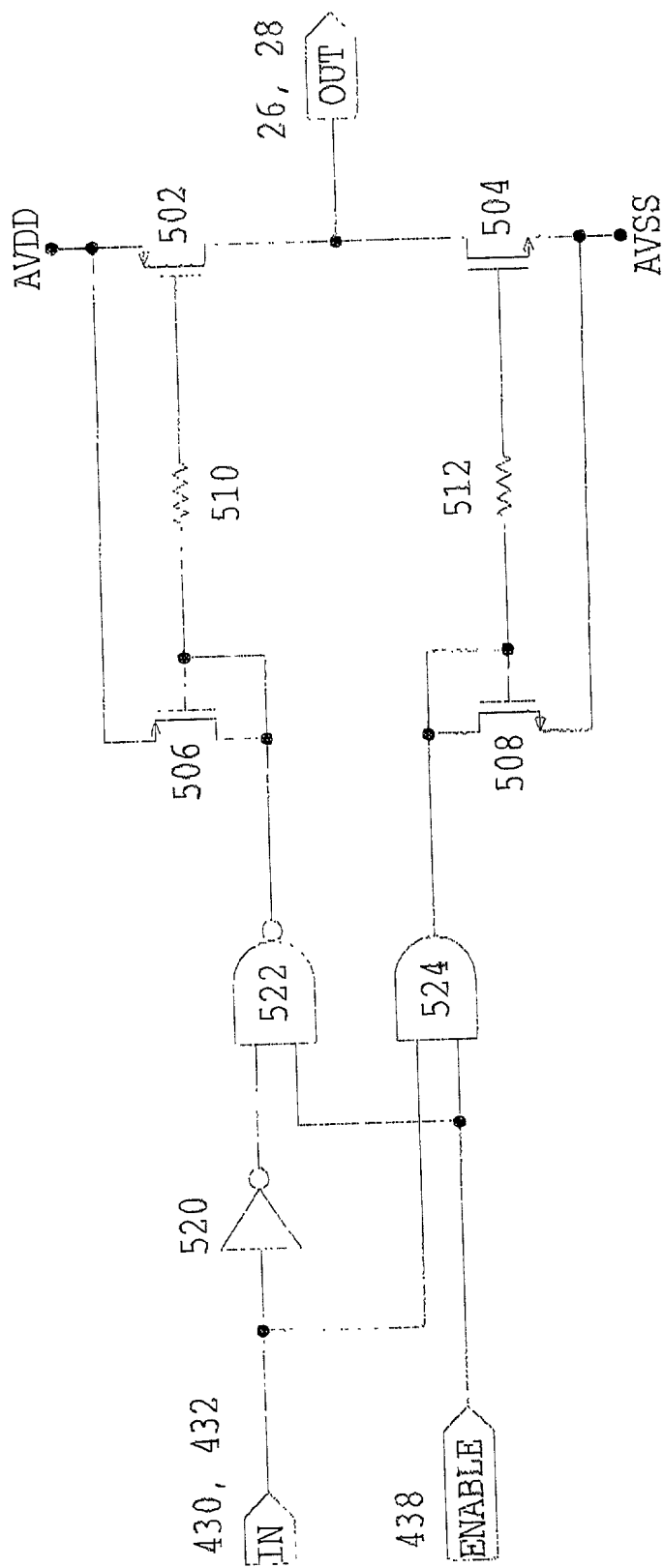


FIGURE 5

Figure 6 is a schematic diagram of a transmitter circuit. The circuit includes a first input signal TXIN_H (36) and a second input signal TXIN_L (38). The TXIN_H signal is inverted by a first inverter (610) to produce a first intermediate signal. The TXIN_L signal is inverted by a second inverter (612) to produce a second intermediate signal. The first intermediate signal and the second intermediate signal are combined by a first OR gate (600) to produce a first output signal. The first output signal is combined with a third input signal TXENA_L (34) by a second OR gate (602) to produce a final output signal. The final output signal is connected to a TXOUT_H (14) output terminal. The circuit also includes a TXOUT_L (16) output terminal. The circuit is powered by AVDD and AVSS supply rails. The circuit includes a first PMOS transistor (700) and a first NMOS transistor (702) connected to TXOUT_H. The circuit includes a second PMOS transistor (704) and a second NMOS transistor (706) connected to TXOUT_L. The circuit includes a first inverter (614) and a second inverter (616) connected to TXOUT_H and TXOUT_L respectively. The circuit includes a TX_LOW signal input to the first inverter (614) and the second inverter (616). The circuit includes a TX_HIGH signal input to the first inverter (614) and the second inverter (616). The circuit includes a TXOUT_H signal input to the first inverter (614) and the second inverter (616). The circuit includes a TXOUT_L signal input to the first inverter (614) and the second inverter (616).

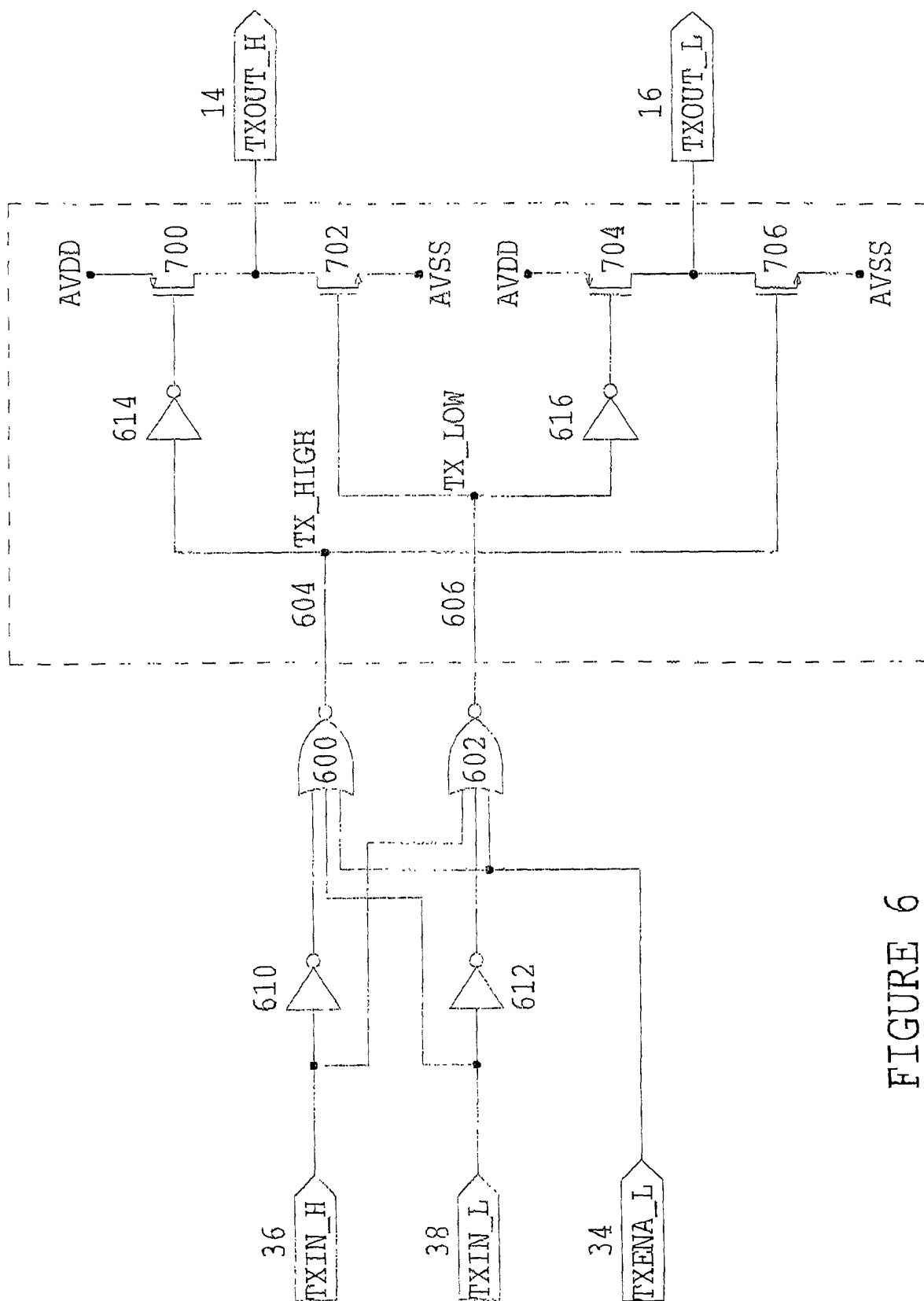


FIGURE 6

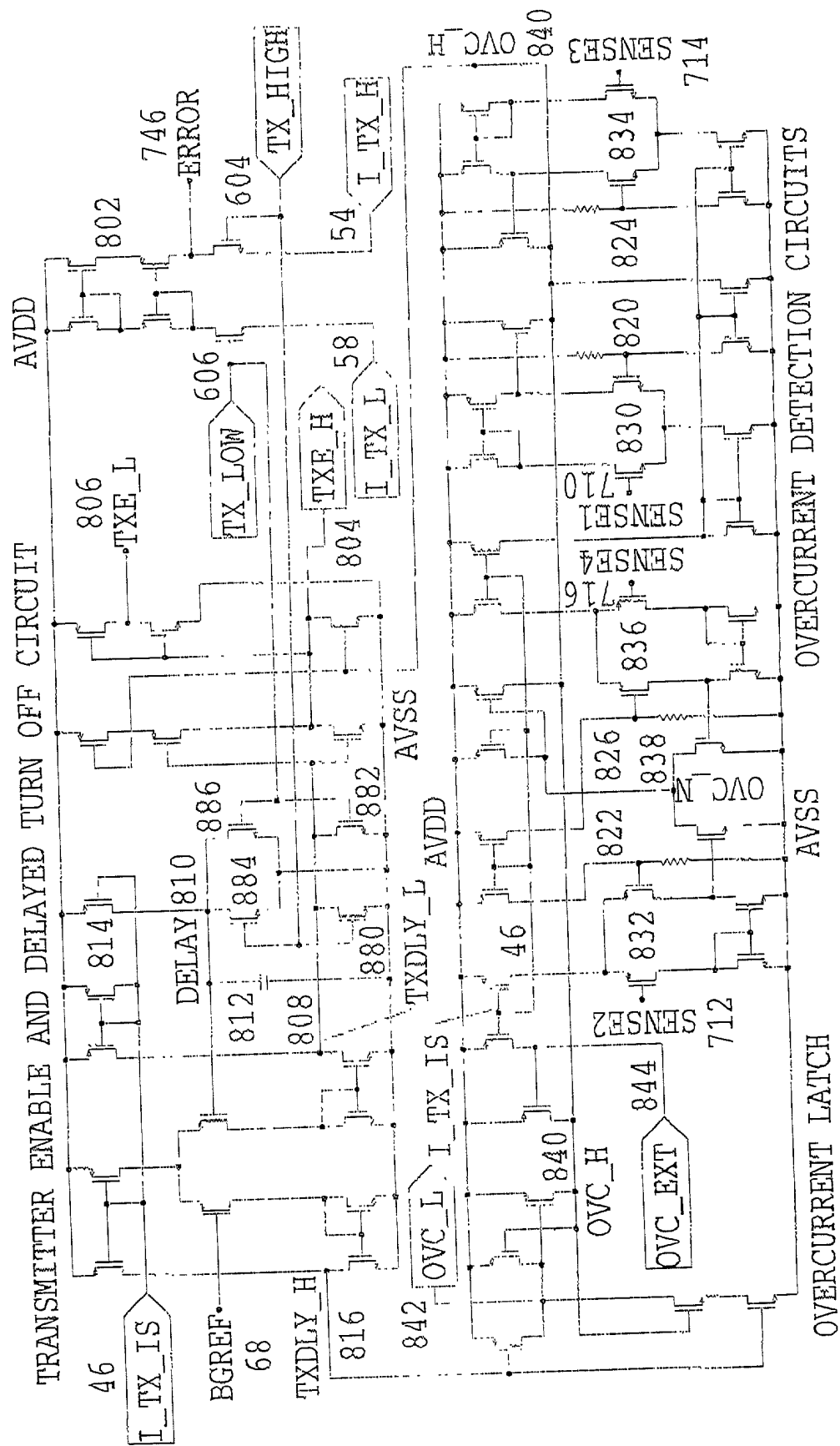
[illegible]

FIGURE 8

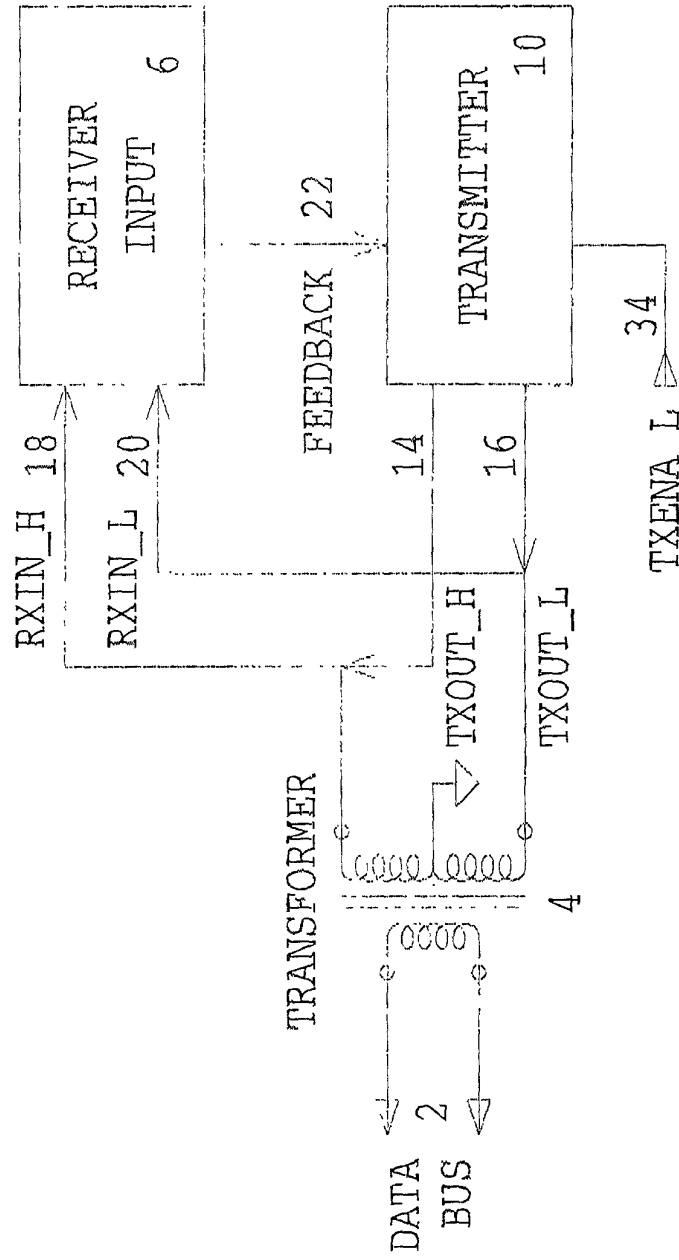


FIGURE 9

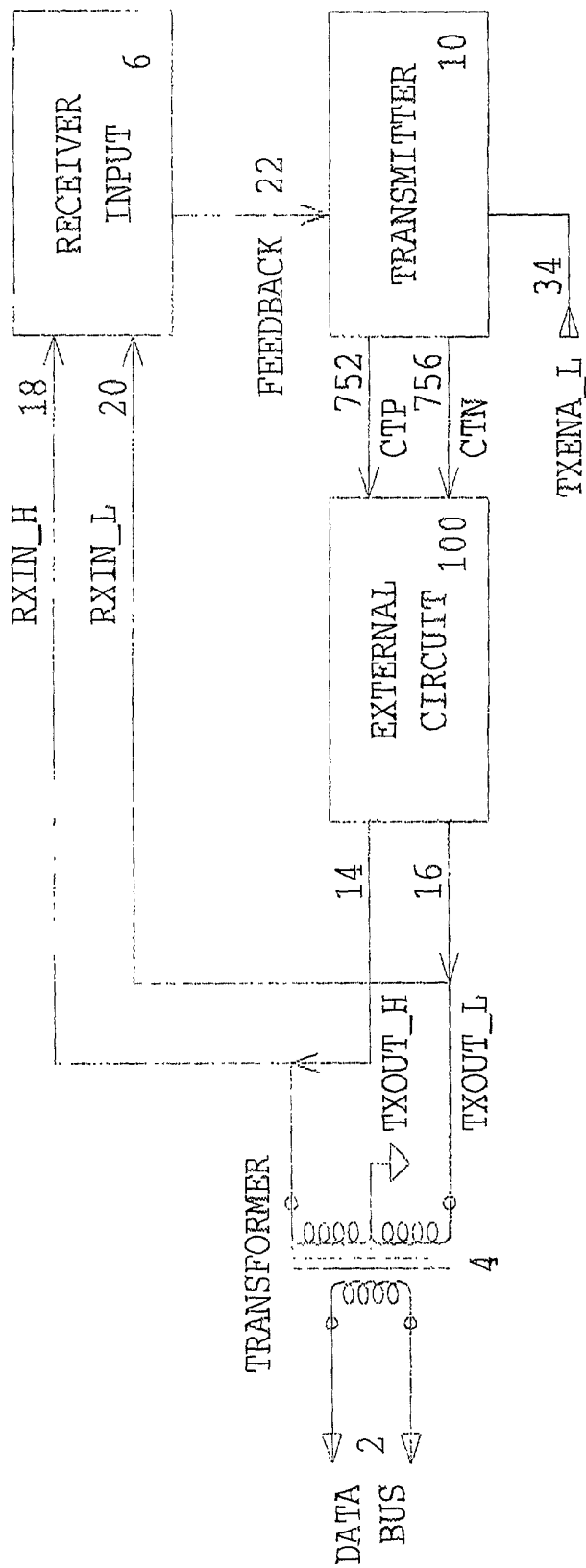


FIGURE 10

FIGURE 11

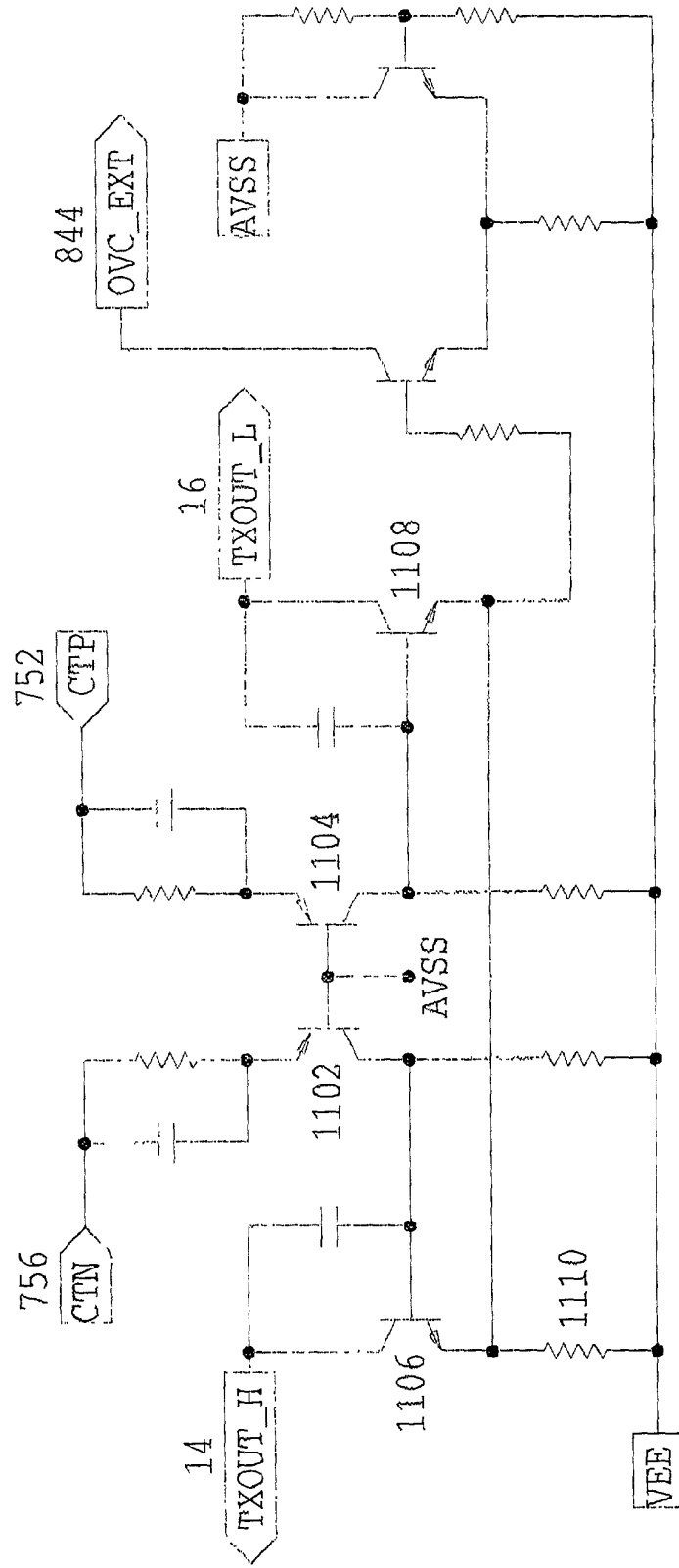


FIGURE 11

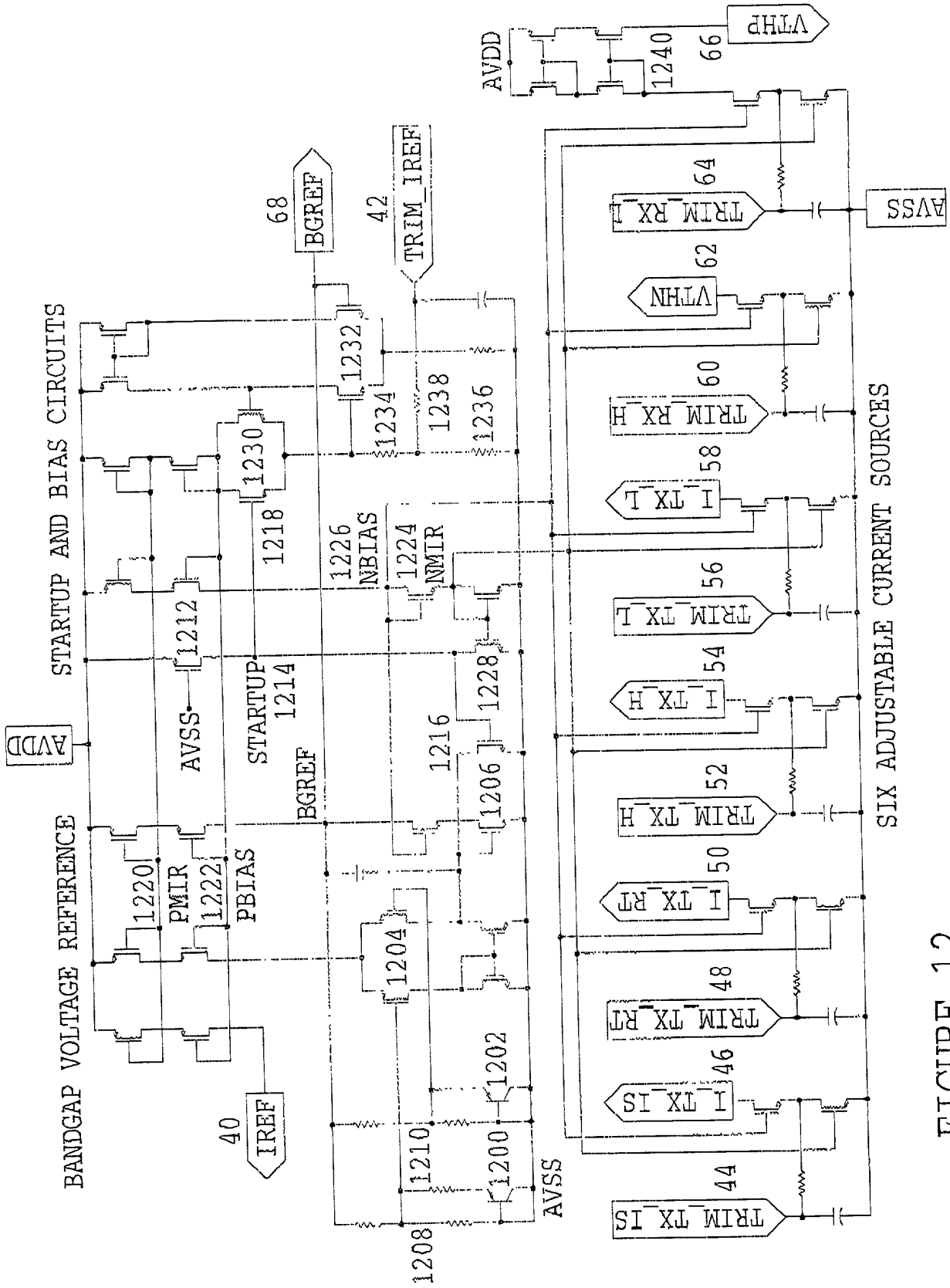


FIGURE 12